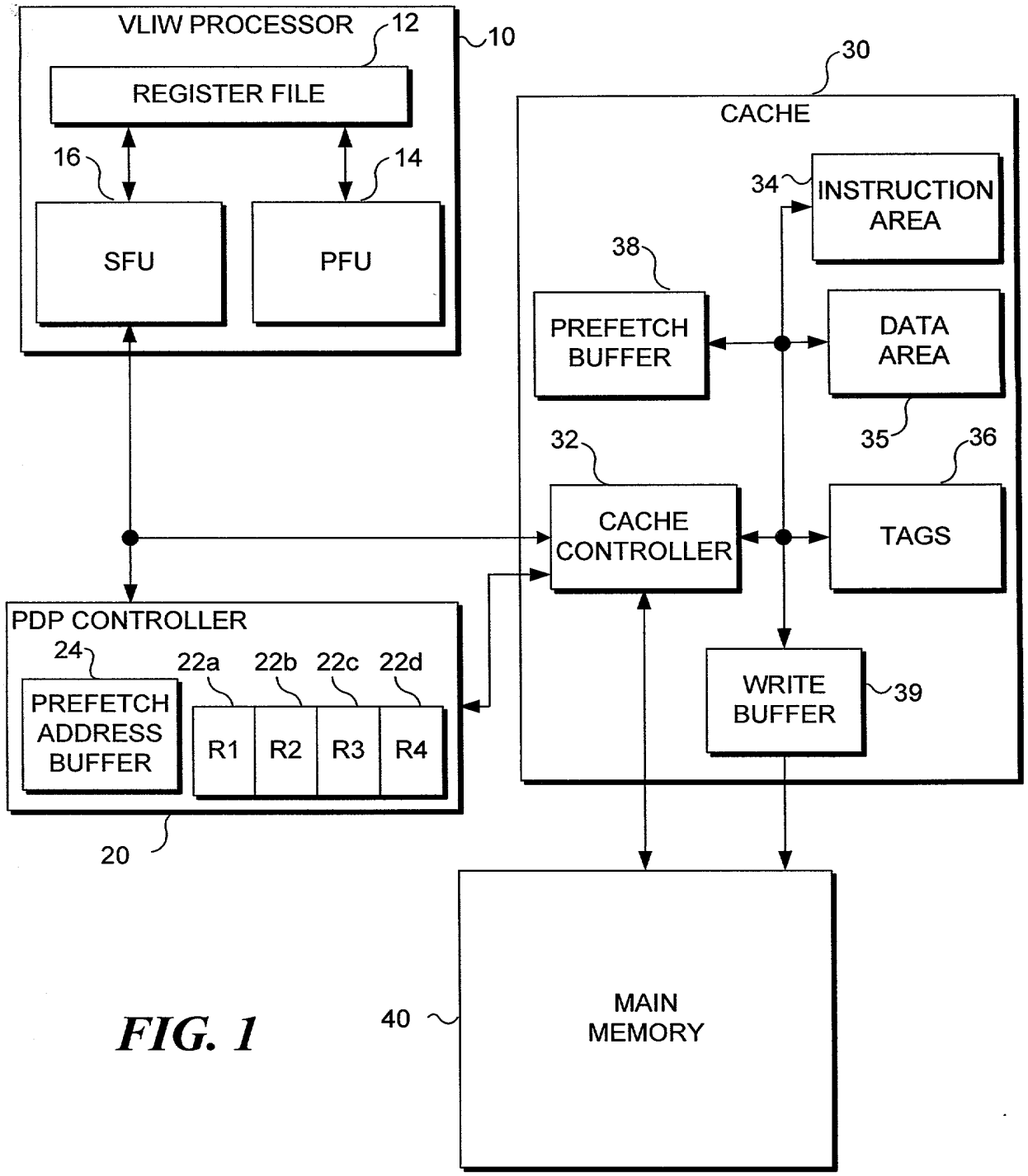

VLIW PROCESSOR
12
10
REGISTER FILE
16
14
SFU
PFU
30
CACHE
34
INSTRUCTION AREA
38
PREFETCH BUFFER
DATA AREA
35
36
32
CACHE CONTROLLER
TAGS
PDP CONTROLLER
24
22a
22b
22c
22d
PREFETCH ADDRESS BUFFER
R1
R2
R3
R4
WRITE BUFFER
39
20
40
MAIN MEMORY

*FIG. 1*

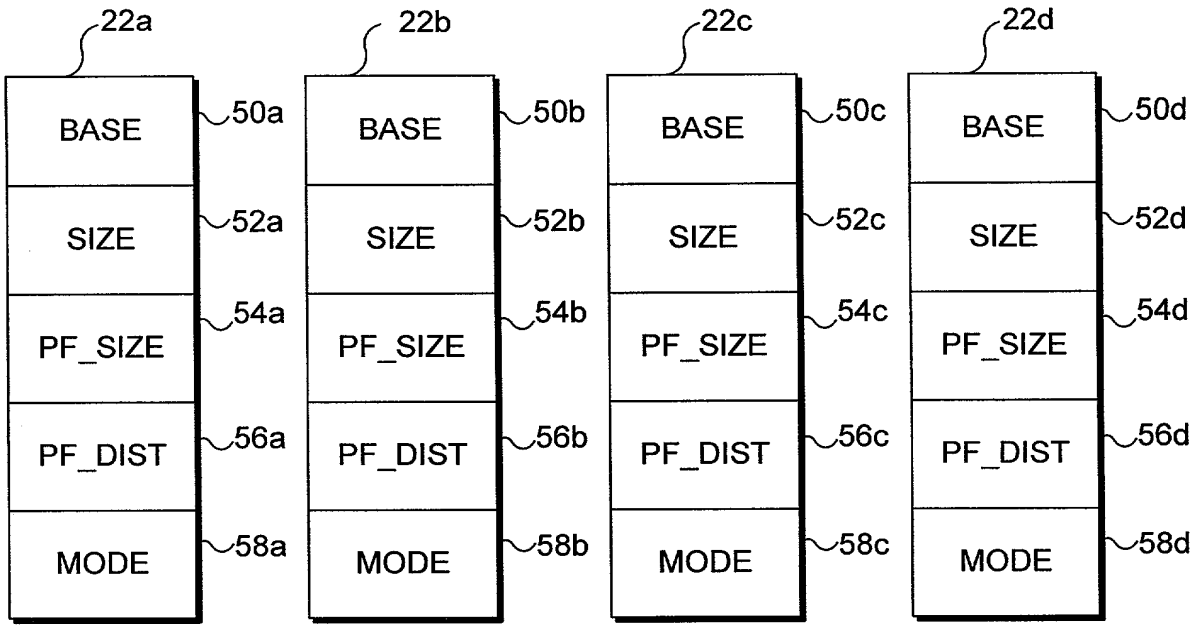



*FIG. 2*

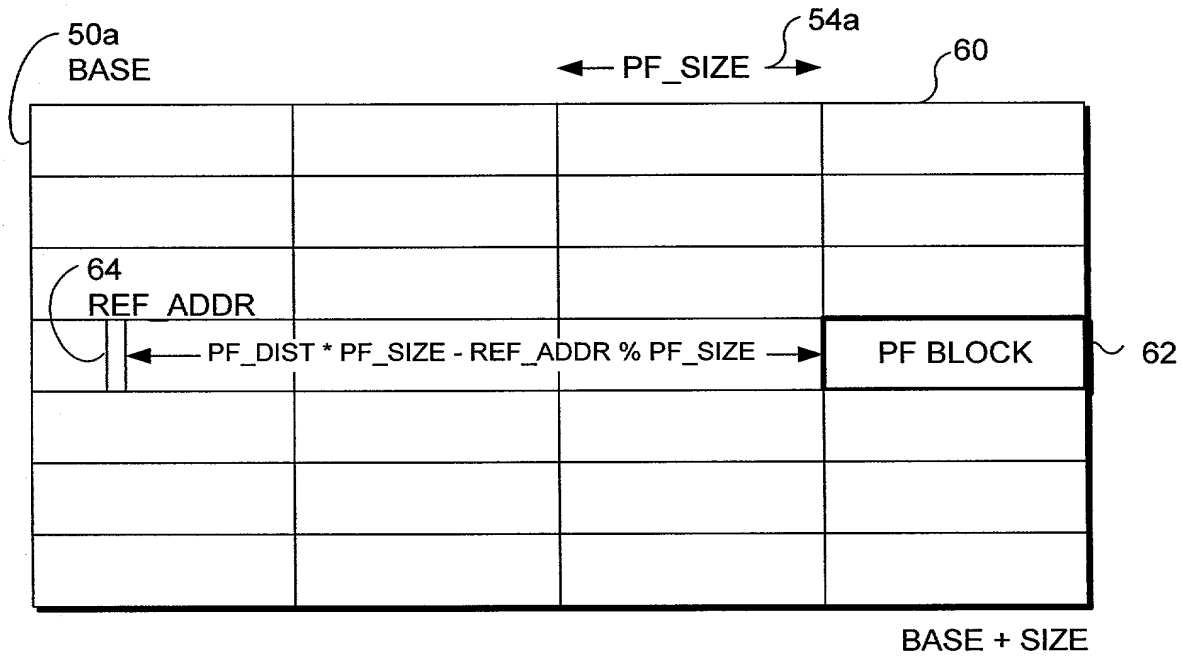



*FIG. 3*

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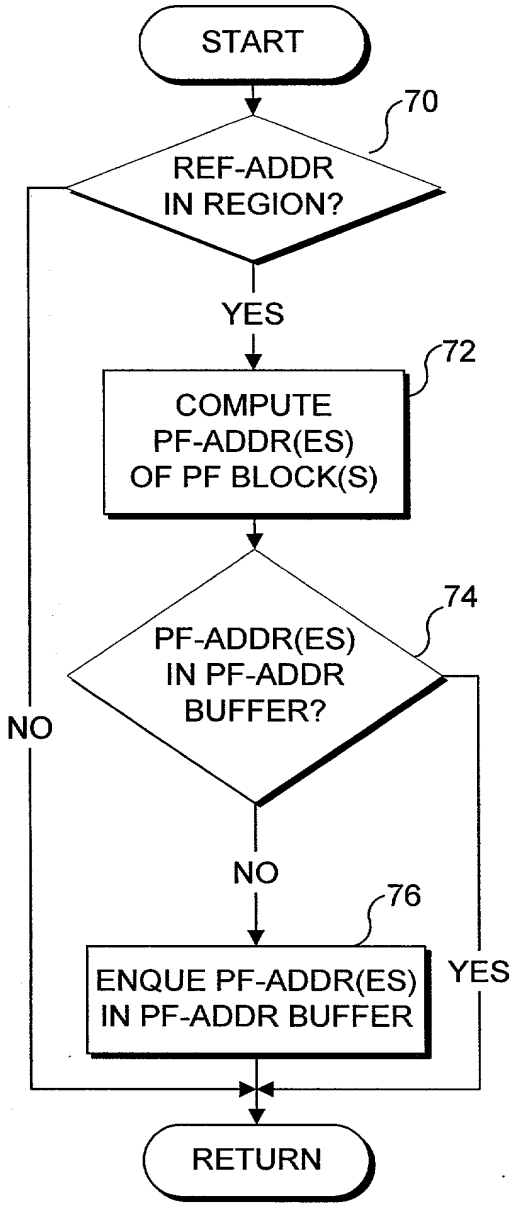

START
70
REF-ADDR IN REGION?
YES
NO
72
COMPUTE PF-ADDR(ES) OF PF BLOCK(S)
74
PF-ADDR(ES) IN PF-ADDR BUFFER?
NO
YES
76
ENQUE PF-ADDR(ES) IN PF-ADDR BUFFER
RETURN

*FIG. 4A*

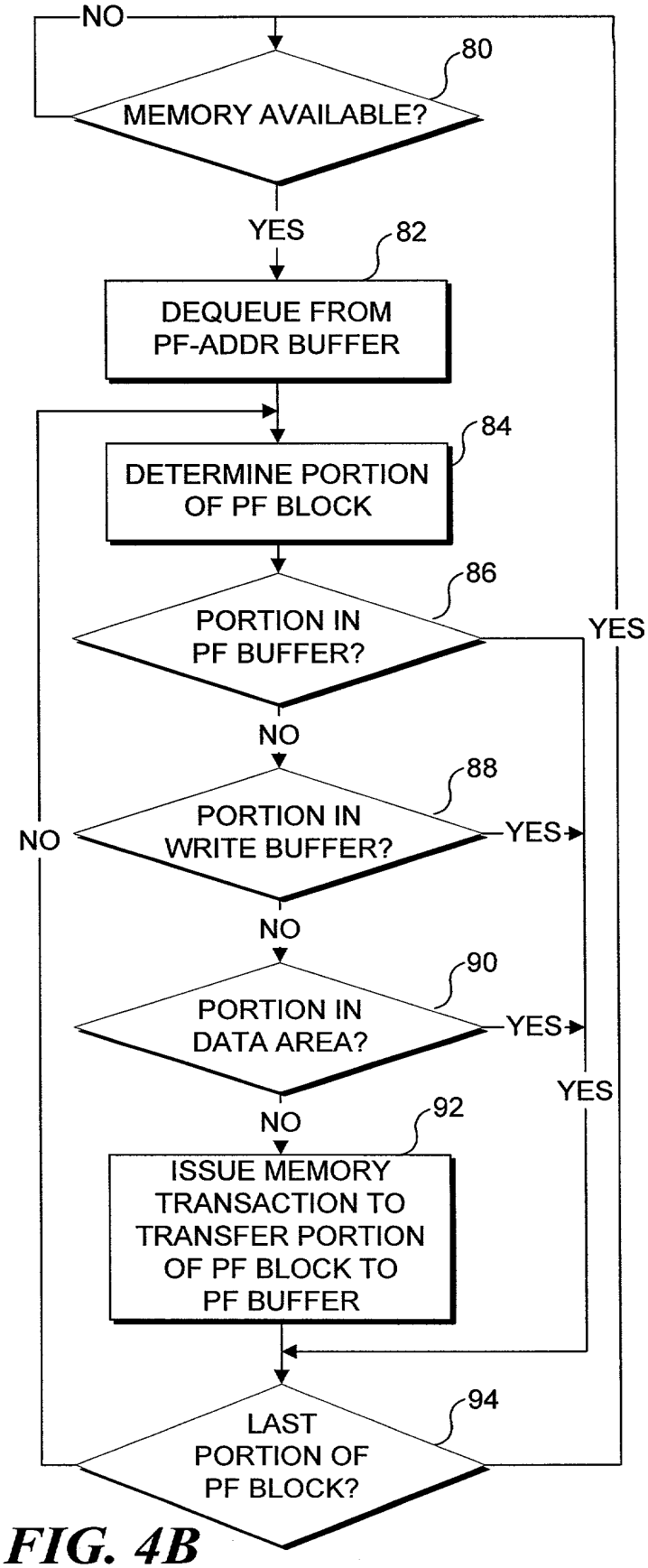

NO
80
MEMORY AVAILABLE?
YES
82
DEQUEUE FROM PF-ADDR BUFFER
84
DETERMINE PORTION OF PF BLOCK
86
PORTION IN PF BUFFER?
YES
NO
88
PORTION IN WRITE BUFFER?
YES
NO
90
PORTION IN DATA AREA?
YES
NO
92
ISSUE MEMORY TRANSACTION TO TRANSFER PORTION OF PF BLOCK TO PF BUFFER
94
LAST PORTION OF PF BLOCK?
NO
YES

*FIG. 4B*

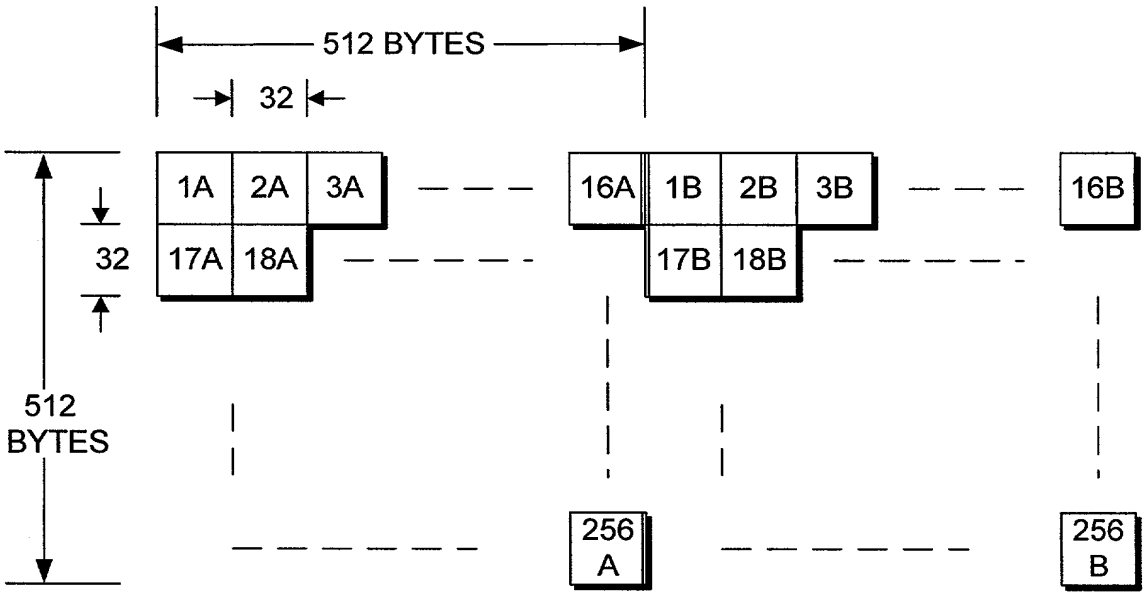

512 BYTES
32
1A
2A
3A
16A
1B
2B
3B
16B
32
17A
18A
17B
18B
512
BYTES
256
A
256
B

*FIG. 5*

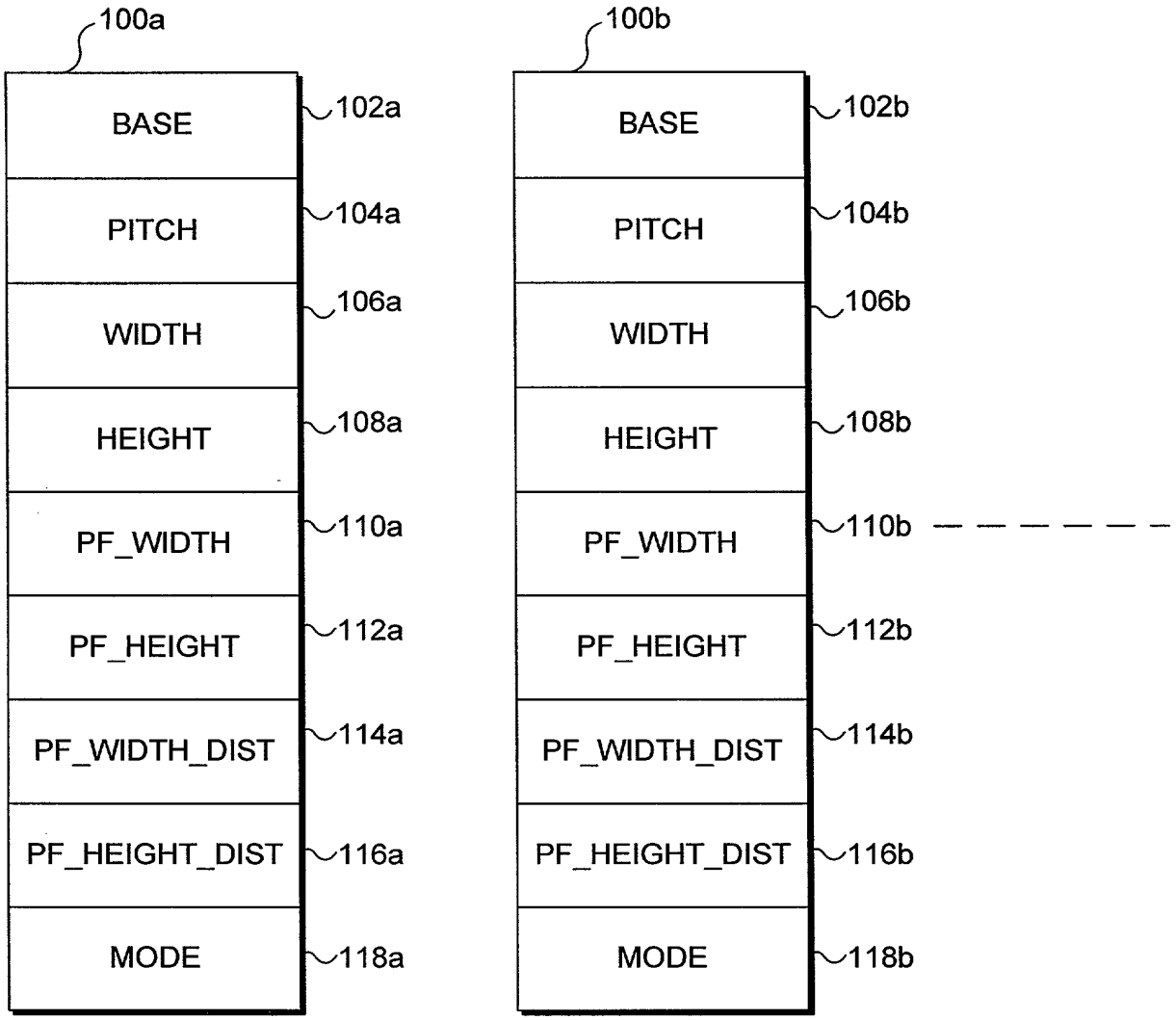

100a
BASE
102a
PITCH
104a
WIDTH
106a
HEIGHT
108a
PF_WIDTH
110a
PF_HEIGHT
112a
PF_WIDTH_DIST
114a
PF_HEIGHT_DIST
116a
MODE
118a
100b
BASE
102b
PITCH
104b
WIDTH
106b
HEIGHT
108b
PF_WIDTH
110b
PF_HEIGHT
112b
PF_WIDTH_DIST
114b
PF_HEIGHT_DIST
116b
MODE
118b

*FIG. 6*

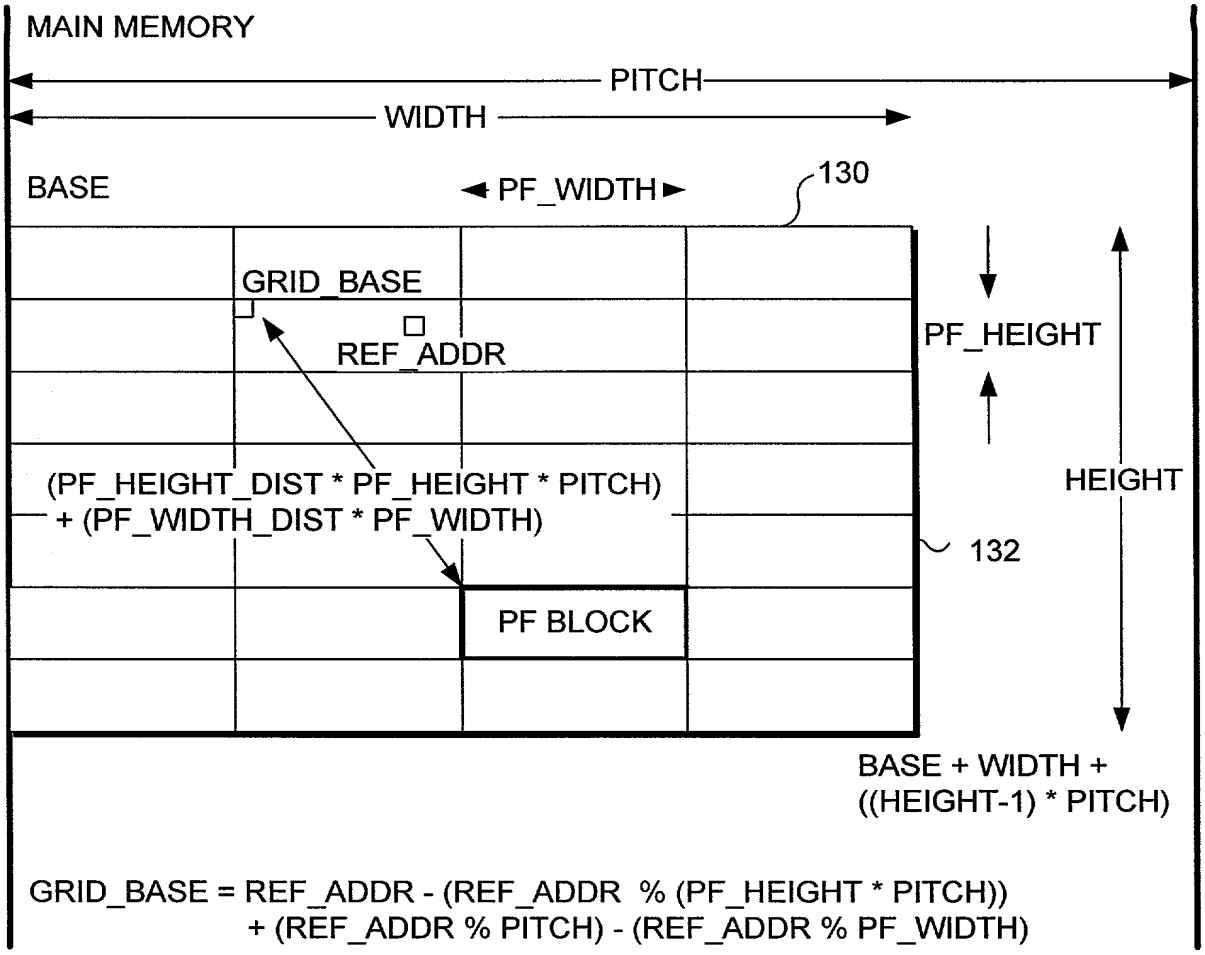

MAIN MEMORY
PITCH
WIDTH
BASE
PF_WIDTH
130
GRID_BASE
REF_ADDR
PF_HEIGHT
HEIGHT
(PF_HEIGHT_DIST * PF_HEIGHT * PITCH)
+ (PF_WIDTH_DIST * PF_WIDTH)
132
PF BLOCK
BASE + WIDTH +
((HEIGHT-1) * PITCH)
GRID_BASE = REF_ADDR - (REF_ADDR % (PF_HEIGHT * PITCH))
+ (REF_ADDR % PITCH) - (REF_ADDR % PF_WIDTH)

*FIG. 7*